



GP 2814

PATENT
ATTY. DKT. NO. AMAT-1931/MD/PVD/DV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Fusen Chen et al.

Serial No. 08/856,116

Filed: May 14, 1997

For: Reliability Barrier Integration for CU
ApplicationAssistant Commissioner of Patents
Washington, D.C. 20231

Dear Sir:

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Group Art Unit: 2814

Examiner: Bernard Souw

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| CERTIFICATE OF MAILING | |
| 37 C.F.R. 1.8 | |
| I hereby certify that this correspondence is being deposited on March 2, 1999, with the U. S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231. | |
| 3/2/99 Date | Keith M. Tackett Keith M. Tackett |

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J. Brun

RESPONSE TO RESTRICTION REQUIREMENT

In response to the Examiner's Action mailed February 4, 1999, having a one-month response period set to expire on March 4, 1999, Applicants provisionally elect claims 1-18 and 20, and request reconsideration of the restriction requirement for reasons discussed below.

THE CLAIMS

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1. A method of filling a hole through a dielectric layer in an integrated circuit, comprising:
 - a) depositing a generally conformal first barrier layer in the hole;
 - b) removing the first barrier layer formed on the bottom of the hole;
 - c) sputter depositing a second barrier layer under conditions of a high density plasma; and
 - d) depositing a metal layer in the hole.
 2. The method of claim 1 wherein the first barrier layer is deposited using chemical vapor deposition techniques.
 3. The method of claim 2 wherein the barrier layer is comprised of Si_xN_y .

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